ИНТЕГРАЛ

588VN1, N588VN1
interrupt controller

Purpose

The 588VN1 microcircuit is an interrupt controller based on planar CMOS technology. The microcircuit is designed to work as part of a microprocessor kit.

Designation of specifications

- bKO.347.367-17 TU

Temperature range

- operating temperature range from - 60 to + 125 °ÿ

Case version

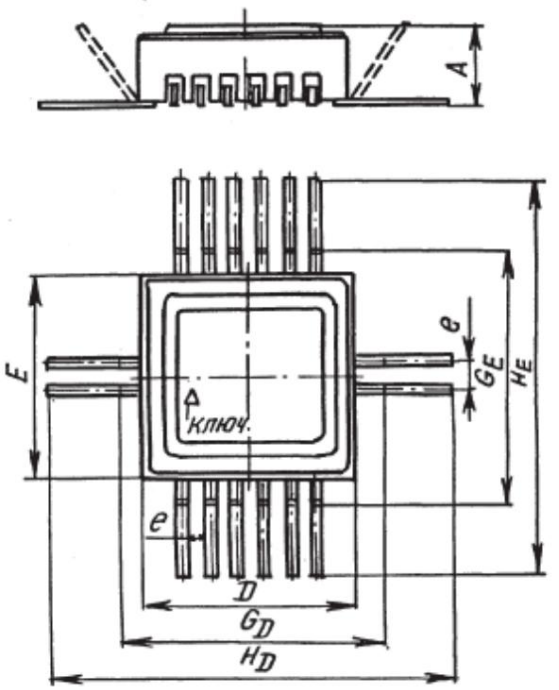
- housing H14.42-1V for H588VN1 •
housing 4119.28-3.01 for 588VN1

Table 1. Main electrical parameters 588VN1 and N588VN1 at Tamb. environment = + 25 °ÿ

Parameter name, unit of measurement, measurement mode	Letter designation	Norm	
		no less	no more
High-level output voltage, V, at Ucc = 5 V ± 10%, IOH = ÿ-0.4ÿ mA, UIH = (Ucc - 0.8) V, UIL = 0.8 V	UOH	Uss-0.4	-
Low level output voltage, V, at Ucc = 5 V ± 10%, UIL = 0.8 V, UIH = (Ucc - 0.8), V, IOL = 0.8 mA	UOL	-	0.4
High-level output current, mA, at Ucc = 5 V ± 10%, UIL= 0.8 V, UIH = (Ucc - 0.8) V, UOH = (Ucc - 0.4) V	IOH	ÿ-0.4ÿ	-
Low level output current, mA, at Ucc = 5 V ± 10%, UIL = 0.8 V, UIH = (Ucc - 0.8) V, UOL = 0.4 V	IOL	0.8	-
High level input current, µA, at Ucc = 5 V ± 10%, UIH = (Ucc - 0.8) V	IIH	-	1.0
Low-level input current, µA, at Ucc = 5 V ± 10%, UIL = 0.8 V, UIH = (Ucc - 0.4) V, High-level	IIL	-	ÿ-1.0ÿ
output current in the “Off” state, µA, at Usc = 5 V ± 10%, UIH = (Ucc - 0.8) V Low-level output current in the “Off” state, µA, at Usc = 5 V ±	IOZH	-	2.0
10%, UIH = (Ucc - 0.4) V, UIL = 0 .8 V	IOZL	-	ÿ-2.0ÿ
Current consumption, µA, at Ucc = 5 V ± 10%, UIH = (Ucc - 0.4) V	ISS	-	200
Signal propagation delay time, ns, at Uss = 5 V ±10%, UIL= 0.4 V, UIH = (Uss - 0.4) V, ÿL ÿ 50 pF	tÿ(WR - AN)	-	140
	tÿ(RD - AN)	-	140
	tÿ(RQINRA , RQINRB-RQINR	-	200

Pin assignment

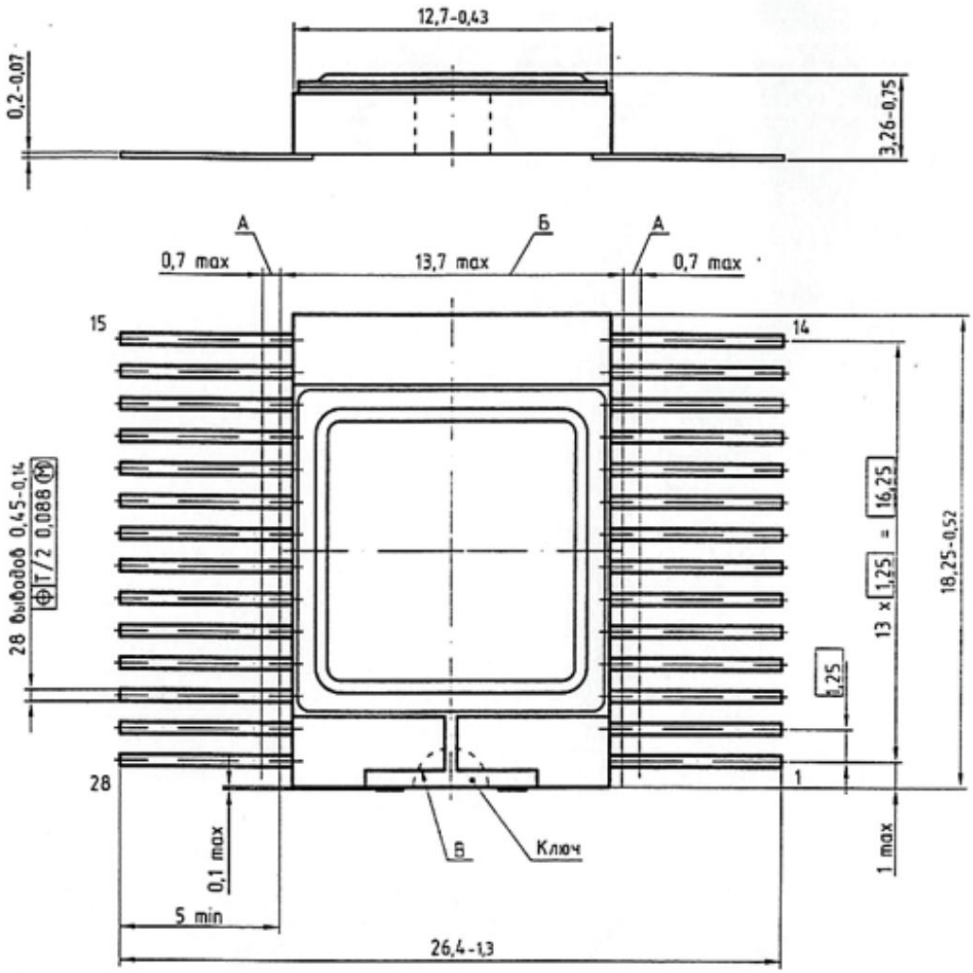
Output	Purpose	Output	Purpose
No. 1	Interrupt vector address input A0	#15	Interrupt grant input INR1
No. 2	Interrupt vector address input A1	#16	Interrupt grant output INR0
No. 3	Interrupt vector address input A2	No.17	Output “Request Interrupt ”RQINR
No. 4	Interrupt vector address input A3	#18	Output “Ready interrupt from external device B ”RAINRB
No. 5	Interrupt vector address input A4	No.19	AN data response output
No. 6	Interrupt vector address input A5	#20	Input ”Initialization” SR
#7	Status register input RGSA	#21	Input/output data address AD0
No. 8	Input “Internal register A” RGA	No.22	AD1 data address input/output
#9	Input “Internal register B” RGB	No.23	AD2 data address input/output
No. 10	Input “Data recording ” WR	#24	AD3 data address input/output
No. 11	Input “Reading data ” RD	#25	AD4 data address input/output
#12	Input “Interrupt request from external devices A ”RQINRA	No.26	AD5 data address input/output
#13	Input “Interrupt request from external devices B ” RQINRB	No.27	AD6 data address input/output
No. 14	Common output 0V	No. 28	Power output from a voltage source U



Корпус	мм			
	D max	E max	H_D max	H_E max
H02.14-1B H02.14-2B	6,8 6,78	6,8 6,78	15,20 14,58	15,20 14,58
H04.16-1B H04.16-2B	8,2 8,08	7,8 7,63	16,60 15,58	15,58 15,58
H06.24-1B H09.18-1B	9,48 9,68	7,88 9,68	17,38 17,58	15,8 17,58
H09.28-1B H09.28-2B	9,66	9,68	17,68	17,68
H14.42-1B H16.48-1B H16.48-2B	12,315 14,50	12,315 14,50	20,215 22,7	20,215 22,7

A -- 3,0 мм
e -- 1,0 мм
G_E -- E max + 1,0 мм
G_D -- D max + 1,0 мм

Figure 1. Dimensional drawing of the H14.42-1B case



1. А - длина вывода, в пределах которой установлено смеще-ие плоскостей симметрии выводов от номинального расположе-ия
2. Б - ширина зоны, которая включает действительную ширину микросхемы и часть выводов, непригодную для монтажа.
3. Нумерация выводов показана условно.
4. Допускается удаление керамического слоя платы в зоне Б

Figure 2. Dimensional drawing of the housing 4119.28-3.01

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http://www.integral.by